BAA 07-24, TRUST in Integrated Circuits (TIC)
Questions and Answers

FAQs dated 3/29/2007

TRUST Industry Day Q & A by category

Teaming

1 Q: We would like to participate in two (potentially competing) proposals. Both SI's are aware of out intentions. Are there any rules or restrictions we should be aware of?

A: No

2 Q: If Phase 1 is dedicated primarily to finding and emphasizing the most promising technologies which may be sourced heavily from "component technology providers," but the contract emphasizes system integrators, will a component technology provider who feels they can focus/perform effectively on their own be at a disadvantage in this process?

A: No, see earlier FAQ question posted on March 21, 2007. If you have a good idea we will not shut the door on you. However, down the road it will be harder to work independently. It will be an issue that will have to be dealt with down the road.

3 Q: Is the government looking for prime/sub teams for technical areas 1 and 2?

A: Would be the most risk free approach.

4 Q: We normally assume "teaming" means prime-sub relationship. Why is this not required?

A: We try not to tell people how to team as a minimum requirement. We have laid out preferences and where we see risk. It is up to you to determine how to handle that risk.

5 Q: Since the SI's will not be known until sometime after the proposal submissions, what sort of teaming agreement is expected if one submits as a technology developer?

A: The teaming agreements aren't meant to be in place between the SI and the technology developer. The relationship does not have to be formalized through a teaming agreement. However, you must state in your proposals that you are able and willing to work with the SI. There must be a free flow of ideas because the SI has certain roles they must perform and cannot be limited.

6 Q: Can you say more about what in a Teaming Agreement contains you are specifically looking for?

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A: The teaming agreement needs to clearly define the working relationship between the members of the team. There must be someone who is responsible for making sure that the interactions between members are working correctly.

7 Q: It is presumed that if the working relationship is Prime/subcontractor then a teaming arrangement is not needed. Is this a correct assumption?

A: Yes

8 Q: For technical providers, what if you pick the wrong system integrator but have a good idea? What if you pick a system integrator and cannot adequately express ideas within a reduced page count of larger (scope) proposal?

A: The technical providers' approaches will be looked at closely in Phase 1 of the program. It should be noted that if the government does not select a bid from a prime, then it can not consider any of the subcontractor s under that bid. The technical provider is allowed to provide separate technology proposal with themselves as the prime contractor and participate as a sub-contractor under another effort; however, it is noted that each submission made that a single performer is team member - either as a prime or subcontractor - will be evaluated on its own merit only (e.g., content/concepts/approaches proposed in one proposal/sub-proposal will not be taken in consideration on another).

9 Q: What examples are there of acceptable teaming agreements?

A: DARPA can offer no specific examples; however, an acceptable teaming agreement must contain, at a minimum, a clear definition of the team structure, flow of ideas/information/data, and member's roles and responsibilities.

10 Q: Can a technology developer submit a proposal as a "standalone" development, or must he be on an SI "team"?

A: You may submit as a standalone proposal; however, you will still be required to interact with a SI increasingly as the program progresses from one phase to another as stipulated in the BAA.

Contracts

1 Q: Will we receive feedback on the results and/or the compromised data back from the metrics team?

A: Yes

2 Q: How many contracts does the government anticipate awarding?

A: The number of contracts to be awarded is based upon the availability of funding.

3 Q: Any cap on phase duration?

A: No; however, as stipulated in the BAA, "Schedule Realism" is one of the evaluation factors to be considered by the Government (Factor 5 - Schedule Realism: The offerors' abilities to aggressively pursue performance metrics in the shortest timeframe and to accurately account for that timeframe will be evaluated.}

4 Q: Any cap on the total duration over all 3 phases?

A: No; however, as stipulated in the BAA, "Schedule Realism" is one of the evaluation factors to be considered by the Government (Factor 5 - Schedule Realism: The offerors' abilities to aggressively pursue performance metrics in the shortest timeframe and to accurately account for that timeframe will be evaluated.}.

5 Q: Can Phase 2 (proposed) be re-submitted based on which outcomes of Phase 1 research are the most promising?

A: The submission of any such re-proposal would be at the Government's discretion based on factors such as the availability of funding, the results of research conducted under the previous phase(s) of the program, general program direction, etc. Please also understand that to be responsive to the BAA, offerors must propose to all phases of the research program.

6 Q: Is there a recommended maximum phase length?

A: No; however, as stipulated in the BAA, "Schedule Realism" is one of the evaluation factors to be considered by the Government (Factor 5 - Schedule Realism: The offerors' abilities to aggressively pursue performance metrics in the shortest timeframe and to accurately account for that timeframe will be evaluated.}

7 Q: Will the government accept/desire proposals that meet only part of the technical objectives for either technical of Areas 1 or 2?

A: Yes - such proposals would be considered responsive to the BAA and would be evaluated accordingly.

8 Q: Is there any restriction on who can be a systems integrator (i.e. companies doing much of the technique work and/or foundry work should be a sub to someone else)? Any limits/restrictions on the number of teams a contractor can be on?

A: There are no restrictions on the teams, members, or leaders.

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9 Q: Will you accept proposals in subsets of Tech Area 1 (e.g. destructive evaluations only) or does a proposal have to address all aspects of Tech Area 1 (non destructive and destructive evaluations)?

A: Yes - such proposals would be considered responsive to the BAA and would be evaluated accordingly.

10 Q: We would like to know if this BAA is considered to have "adequate price competition" and, if so, confirm that we are not required to submit a TINA-certified proposal.

A: DARPA requires a TINA-certified proposal as offerors are not proposing to a common statement of work/SOO. Upon completion of negotiations with those selected, the PCO will request a Cost/Pricing Certification be completed.

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TRUST Industry Day Q & A by category

Test Articles

1 Q: Will the process monitors be made available as GFE? Will the process monitors for the gold standard be made available?

A: No, the process monitor data is proprietary to the foundry. Some parametric data about that particular run will be made available on the MOSIS website.

2 Q: How will the test article team identify and distinguish clean/gold chips versus altered chips? (e.g. will they just print a number on the external package or burn in a key/number?)

A: The test article team will generate a unique identifier for each design type.

3 Q: Can the performing organization do the design of test articles?

A: Only that test article team will design the test articles. However, if an approach is reliant on a particular design feature to ensure TRUST then the test article team will work together with the performer to incorporate any design alterations required.

4 Q: Will the test article team explicitly tell participants when they are receiving altered test articles?

A: No, not for the Go/No-go experiment. However the government will reveal any modifications to the test articles provided in the sample test article set that will be provided in the early months of the program.

5 Q: Will the Trojans inserted create or result in logic errors (i.e. there are no Trojans that create transient defects or latent defects).

A: Yes, the Trojans will result in logic errors. Reliability issues are not in scope of the BAA.

6 Q: If "special circuits" are being added at contractor(s) request, will the information be distributed with the ICs? If not, will the contractors receive ICs without special circuits unless they have requested something?

A: Yes. If an approach requires special circuitry, that contractor needs to state their requirements in their proposal.

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7 Q: Will malicious insertion actually intend to achieve an adversary objective? What is interest in prevent/detect the objective?

A: Malicious insertion will prevent the ICs from properly functioning. Any approach that will prevent or detect such an attack is of interest.

8 Q: If our approach inserts circuitry, are we exempt from dealing with Article 0?

A: Test article 0 is provided for the bidders to get a baseline on their performance. Test article 1 is the first official milestone.

9 Q: Will it be possible to obtain multiple gold standards and multiple bad ICs for non-destructive evaluation?

A: Yes, 10 will be provided. More can be requested.

10 Q: The 1st Test Article indicated that it will contain the malicious circuits in the Physical Design. Can we also obtain Logic Design Trojan Horses?

A: Yes.

11 Q: Is the gold standard circuit going to be defined by DARPA?

A: Yes.

12 Q: Are the circuits in 90 & 65nm node?

A: Yes.

13 Q: Can I use Altera parts for phase 1 test articles?

A: Yes.

14 Q: Will the test article evaluations take place in the 10th month of each phase regardless of contractors specified phase length?

A: The test articles are planed to be available in the 10th month. This can be modified depending on the phase length proposed by the contractor.

15 Q: How does the number of transistor estimates translate into area? What approx area per transistor can be assumed?

A: The current plan for test article 1 is to use the IBM 90nm SF or RF processes please refer to the IBM website.

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16 Q: How many metal layers are estimated for each phase? Can we start smaller and grow over program?

A: Please review the IBM website for specific details.

17 Q: Can we assume that the foundry does not modify the design except for adding malicious circuits? Can identifying non functional changes made by foundry for manufacturing be addressed incrementally over program?

A: Manufacturing changes will be present in each test article. The performer's approach will need to account for the relevant non-functional changes needed for manufacturing..

18 Q: How do you expect to catch anything if the design is faulty – What to compare against? Comparing against problem spec will not work – malicious action can be effected by a secret input to IC.

A: The Test Article Team will provide a gold standard for comparison.

19 Q: Our solution requires changes in the original RTL of the test circuit. Whose job is it to finish the design process starting with the modified RTL?

A: The contractor will need to work in partnership with the test article team.

20 Q: What are the deadlines for submitting design features to be added into the test articles?

A: It is scheduled for 2 months before tape out.

21 Q: Some commercial tools already do equivalence check (semantic) between bitstreams and RTL. What does the FPGA program expect to do in addition?

A: The proposers must determine what they must do to meet the goals and requirements of the BAA.

22 Q: Will DARPA provide access to CPU cores and/or design tools (for "testing and evaluation" only) to COTS/FPGA projects? Or will all such proposers have to license those things individually from commercial vendors?

A: No. The proposers must license the tools and cores from the vendors.

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TRUST Industry Day Q & A For Metrics

Metrics

1. **Q: If we have a good idea for prevention but are weak on detection, our P_D won't look good for the whole IC. Is this acceptable?**

A: Yes; but please clearly address how you arrive at $P_{Prevention}$ and $P_{FalsePrevention}$ numbers.

2. **Q: Are there target results for $P_{Prevention}$ & $P_{False\ Prevention}$?**

A: The goals for $P_{Prevention}$ and $P_{FalsePrevention}$ are currently not fully defined. However, they should be close to or the same as the detection goals presented in Table 3. Your proposal should address the goals you plan to achieve, the utility for achieving these goals in light of rogue transistor insertion threats to modern ICs at 90 nm and below node size, and the method used to arrive at the $P_{Prevention}$ and $P_{FalsePrevention}$ statistic.

3. **Q: Since metrics will evolve during the program with inputs from metrics team, will the metrics team be available to help in the proposal stage to create appropriate metrics from the start?**

A: It is inappropriate for anyone on the government team to be involved in any proposal effort. Initial metrics for the program have been established; see Table 3. Your proposal should address achieving these or like goals to the best of your ability.

4. **Q: Time to evaluate metric question! Time to accomplish what? 1 chip, 1 wafer, etc? What if the setup time is large (e.g. signature vectors) but chip test time is short?**

A: This is the time to reach a decision regarding TRUST in and IC including set-up time.

5. **Q: Obfuscation is qualified by a "probability of prevention" (mentioned in 1st question section). Can you elaborate on this with an example? How do P_D and P_{FA} apply to modified FPGA bitstreams out of tools?**

A: See Question 2 above. Your proposal should address how P_D and P_{FA} relate to a modified FPGA bit stream. One possible method, however there are many others, might envision the modified bit stream as a modified hardware configuration that can

be compared with the original "gold standard" bit stream design. Thus an equivalent P_D and P_{FA} measure might be derivable.

6. Q: Will Dr. Wilt's probability analysis be available to the proposers?

A: The extended abstract from Dr. Wilt's recent GOMAC presentation can be obtained from GOMAC, but does not directly relate to the BAA. However, Dr. Wilt's presentation from the Industry Day will be available.

7. Q: Does the metric for "time" reflect the total time from a Systems Integration point totaling all individual components to 480 man hours?

A: The time metric applies to all techniques (individual components) that the SI manages together. Also please see the answer to Question 4 , for the definition of "wall clock" plus "man-hour" time.

8. Q: If new metrics are proposed, how tightly do they need to be bound to the BAA metrics?

A: They need to be "tightly" related or thoroughly explained if different. The program strongly endorses the use of P_D, P_{FA} and Time as metric measures for IC's of the given density and node size.

9. Q: For P_D tables do you need to define specific threats that are being detected?

A: No

10. Q: Regarding "information leakage" where the goal is to hide intent, the metrics established (P_D and P_{FA}) don't apply. Is there a plan on how to test and apply metrics to this type of proposed solution?

A: Your proposal should address achieving P_D and P_{FA}-like goals to the best of your ability. If you believe that the P_D and P_{FA} metrics presented in Table 3 do not apply, you should clearly explain your rationale for not using these as well as the basis for any metric measures that are substituted.

11. Q: Assuming a trusted FPGA fabrication the trust metrics don't seem to apply. Would some type of bit-level configuration P_D and P_{FA} be more applicable? Please clarify between low-level and IC-level metrics.

A:. We believe that this question is in essence asking whether the configuration bits in the FPGA could be considered "transistors" for metrics purposes for Area2/Case3. If we are interpreting this question right, the answer is potentially yes, however, the proposed metric and program goals should be thoroughly explained in the bidder's proposal. The metrics presented in the BAA on Table 3 are "transistor" level metrics.

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12. Q: The phase definition seems to suggest mostly SI work in Phases 2 and 3. However, the metric improvement is assumed to occur throughout all 3 phases?

A: It is envisioned that development leading to improvement in performance at the technology component level will continue in parallel with System Integration efforts during Phases 2 and 3. However during these phases, the component technology developer may need to maintain a teaming relationship with the SI in order to ensure continued applicability and transition of technology.

13. Q: Regarding gate level metrics versus transistor level metrics. If we propose gate level or standard cell level metrics for P_D and P_{FA}, how will these be viewed in light of other proposers who might use transistor level metrics? Is there any midpoint to the selection criteria? What are the impacts?

A: Since a gate can have a variety of transistors and other devices, any gate level metrics should be converted to transistor or device level metrics so that the goals specified in Table 3 can be preserved and used for comparative purposes.

14. Q: A transistor is not a unit of measure for FPGAs, EDIFs, or bitstreams and the mapping of bitstream features to actual FPGA IC transistors is not a publicly documented feature. How do we get back to a transistor based P_D and P_{FA} number for FPGAs? Does it even make sense to do so? In the case of FPGAs, would it not make more sense to value P_D over P_{FA}, since the cost of throwing out a bitstream is much less than the cost of throwing out an ASIC?

A: It is understood that the internal design of COTS FPGAs are not available to performers. In the case of an FPGA it is anticipated that the performer will relate the FPGA programming to a transistor-level equivalent. One possible method, might envision the modified bit stream as a modified hardware configuration that can be compared with the original "gold standard" bit stream design. However, there are many other methods that can be used. Thus an equivalent P_D and P_{FA} measure might be derivable. On the question of valuing P_D over P_{FA}, the program goals are specifically stated in terms of one point on the ROC curve.

15. Q: Why is P_{FA} defined to include transistors in a circuit that was correctly detected bad – should refer to good circuits falsely classified as bad.

A: You are correct. If a circuit is called "bad" and it contains rogue transistors then there is no P_{FA} associated with the circuit. However, if the circuit was called "bad" and there were no rogue transistors in the circuit then the entire circuit logic would contribute to the P_{FA} number (in the case of the example, this would be 2048 transistors that were falsely classified).

16. Q: It appears a technique that is perfect at the IC level is unduly penalized because by the defined metrics it has a transistor level P_{FA} near 100%. Please reconcile.

A: It appears that the intent of this question is the same as the previous one – if there is a technique which operates perfectly at the IC level (100% detection of altered ICs, and 0% false alarms on good ICs) the example seems to suggest that the transistor P_{FA} is nearly 100% since valid transistors are classified as false alarms in either case. A correct assessment of an IC-level technique would only count transistors as false alarms in the case where a false-alarm decision is made at IC-level. In order to generate an accurate assessment of the transistor-level false alarm rate in the case of this technique, multiple ICs would have to be tested and the transistor-level false alarm rate could be defined by averaging across a group of tested ICs.

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FAQs dated 3/26/2007

Q: Regarding the use of P_D and P_{FA} to create ROC curves. A single experiment to try to identify a fault (malicious circuit or design) will result in 1 datapoint. How are you expecting a ROC curve to be generated? It would appear that many experiments using the same identification and fault mechanisms are needed for a curve, but the testing plan (Fig 15 pg 25) does not show this. ROC is discussed for example at http://en.wikipedia.org/wiki/Receiver_operating_characteristic, where $0<P_D<1$ and $0<P_{FA}<1$ but your examples (pg16-17) seem to show that PFA~0 in all cases. Please elaborate on the ROC curve you expect using your examples.

A: We are not expecting the participants to generate an exhaustive set of ROC curves, rather to demonstrate achieving the measurable "point" P_D and P_{FA} goals that are shown in Table 3.

Q: Regarding the use of P_D and P_{FA} for FPGAs The examples (pt 16-17) use transistors to measure faults, and pg 17 suggests using equivalent gates/transistors when measuring FPGAs, and somehow identifying the contents of built-in hardware. This does not appear to be practical. Since different FPGAs use different architectures, what about instead measuring bits in the configuration bitstream instead of transistors? This measures all user-specifiable content, but does not include hard-wired hardware.

A: Other measures will be acceptable so long as they result in quantifiable P_D and P_{FA} metrics for experimental results that demonstrate performance equivalent to the program goals that are shown in Table 3.

Q: Regarding faults in FPGAs. Will a golden reference be available for FPGA tests?

A: Golden reference models will be available. This could include RTL and netlist views for the design and or IP dependent on the experiment.

Q: Regarding functional verification of malicious circuits. Does the malicious circuit match with the specification? Are testbenches delivered, or do we have to generate these from the specifications? What type of specs are delivered?

A: Test benches will be delivered with all test article circuits. There will be specifications provided as well. These specifications will be the standard documentation set needed for use of the circuits.

Q: Regarding testing verifiable-by-design FPGA circuits. All the test articles (Fig 15 pg 25) appear to be arbitrary circuits containing faults. We are interested in generating circuits that are verifiable-by-design, as opposed to verifying arbitrary

circuits. It does not appear that the testing plan supports a verifiable-by-design methodology. A plan that would support it would allow us to generate the FPGA circuit, have the attacker modify it, and we would detect any changes.

A: The program schedule allows for a performer to insert circuits into the test article design for an experiment that will evaluate their technique.

Q: Regarding substitute FPGAs. The test articles (Fig 15 pg 25) do not appear to cover the use of substitute FPGAs with modified malicious functionality. Is there a plan on how to test hardware-fingerprint mechanisms, or is this a test we need to design and implement?

A: Amended Answer: The FPGA test articles will not contain malicious hardware modification or modified malicious functionality that is caused by hardware modification during manufacture. If a technology offered deals with hardware-fingerprint mechanisms that require hardware modification then this will be covered as part of the Case 1 ASIC verification area. If a technology offered deals with programmable hardware-fingerprint mechanisms, then this will be covered in test article generation for the Case 3 area. For the FPGA Case 3, the test's focus is on the detection and prevention of malicious behavior in the uploaded test article design not the physical FPGA hardware. Additional tests may be proposed as long as they meet the defined performance goals.

Q: This question pertains to teaming agreements and the definition of "success" within Technical Area 1. You state that "technology proposals that require multiple companies participating to succeed must have a teaming agreement, even in Phase I".

In this context, does *success* refer to a complete Tech Area 1 solution (for instance, a proposed destructive evaluation solution, and a proposed non-destructive evaluation solution, along with risk reduction approaches, systems engineering etc)? Or, does success refer to individual technology components within Tech Area 1 (for instance, a complete destructive evaluation solution only)?

A: "Success" refers to the final goal of the TRUST Program as it relates to quantifying the TRUST of an IC. With regard to your specific question, for instance in the area of destructive or non-destructive evaluation, the final goal is to determine the level of trust for an and-to-end capability when using either destructive or non-destructive methods. The overall capability may be comprised of several intermediary steps that may rely on data or products produced at each of the intermediate processes. However, the overall program goals are satisfied by integrating these intermediary steps together. If more then one company possesses the parts of the required end-to-end process then the government would prefer that these companies enter into formal teaming agreements, submitting one consolidated proposal to best address the capability being offered..

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Q: Explain what Combined man hours plus wall clock time means on Table 3.

A: This is the amount of effort in terms of time taken to determine that an IC can be trusted. A fully automated approach would only expend an amount of time equivalent to the interval between receiving the IC to be evaluated and making the decision of its trustworthiness. This is the minimum time that any evaluation effort could take. We are referring to this interval as "wall clock" time. If however, one used a completely manual process, the time expended would be measured in the amount of "man-hours" taken plus any down time then people were not working. If more then one person worked over the same interval, there would be an increase in man-hours required.

Example 1: Completely automated process that takes 10 days; Combined man hours + wall clock time = 0 man-hours +240 hours of automated processing = total time of 240 hours.

Example 2: 1 person using manual effort for 8 hour/day over 10 days = 80 man hours + 160 hours clock time when he/she was not working = 240 hours

Example 3: 3 persons using manual process for 8 hours/day over 10 days = 240 man hours + 160 hours of clock time when they were not working = 400 hours.

Example 4: 2 persons working a manual process 8 hours/day plus 8 hours of an automated process each day for 10 days = 160 man hours + 80 automated processing hours + 80 hours of clock time when not working = 320 hours.

Q: Will the ASIC have JTAG scan access to all registers within the device?

A: No

Q: Are the Test Artcle ASIC's device packages the same for all 3 phases of the program?

A: No

Q: Is the same FPGA device type used for all 3 phases of the program?

A: No

Q: Does the Hardware Validation Technical Area 1 include FPGA's? If so, will there be trusted and untrusted test articles of FPGA's for this hardware verification?

A: No

Q: The BAA states (p18): Test Vectors—Test vectors are a complete suite that validates functionality and performance of the design.

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- **What is the above meaning of "complete"? Is completeness defined with respect to a set of defects/faults?**
- **For example, will the "complete" vectors for the Bridge circuit in Fig. 9 detect the change introduced by Circuit 1 in Fig. 10?**
- **Are these vectors supposed to be trusted?**

A: The vectors will be complete relative to the specification provided. Vectors are to be trusted in some cases.

Q: The test articles include RTL. If our solution requires to change the RTL by inserting additional logic for TRUST, whose job is to finish the design process starting from the modified RTL?

A: It will be a partnership with the test-article team. The test articles are designed to handle multiple insertions into the logic.

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Q: What is the preferred group/grant size?

A: The preferred group size and amount proposed is up to each individual proposer and related to the scope of the work they propose. Due to security concerns with this program, there will be no grants written.

Q: Are there any efforts to help connect groups?

A: There are two opportunities to for potential proposers to meet up with potential teaming partners. The first in the Industry Day, the details for this are available on www.fedbizopps.gov and the second is the teaming website, with is https://www.davincinetbook.com/teams.

Q: When/where (time and exact location) is the meeting (to purchase the plane tickets)?

A: The Industry Day is will be March 26, 2007 in Arlington, VA. More details on this meeting are available at www.fedbizopps.gov (SN07-24, Posted March 16, 2007).

Q: The second part of the BAA stresses detecting inserted logic while the first part emphasizes methods to prevent reverse engineering. Is the desired focus exclusively in the area of detecting malicious logic like the examples? Is this the intended shift in focus from the first BAA that is being reissued?

A: This BAA is completely separate from BAA06-40 and that solicitation has been closed. The focus of this solicitation is on the detection and prevention of added logic in ICs.

Q: The proposal submission does not seem to have white papers, just full proposal. Do we need to have the full proposal by 23 April? Can we send the more traditional 5 page white paper? If there is interest by MTO, we can send a full proposal afterwards.

A: To be considered in the first and potentially only round of considerations under BAA 07-24, your full proposal will have to be submitted by April 23, 2007. No proposal abstracts will be evaluated under this solicitation.

Q: Does DARPA desire that the System Integrator (Prime) submit the sub-contractor technical proposals to show an integrated approach to "Trust" rather then have the individual technical proposals submitted separately? Does the Prime attaching the more thorough technical proposal as an addendum suffice in order to show the breadth and depth of the efforts and feasibility of the research being done?

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A: In the case of an effort with the prime contractor and sub-contractor relationships identified, it is desired that the prime contractor submit only one proposal for the effort.

Q: Case 3 involves FPGAs whose content is not determined until a bit pattern gets loaded after they are installed on a board and who's contents are subject to modification after the initial configuration is loaded. Does DARPA intend for the scope to cover techniques that will ensure that original code got loaded and to prevent modifications to the original code (using techniques such as encryption, signature analysis etc.)?

A: Techniques that ensure that the correct bitstream is loaded are within the scope of this BAA.

Q: The actual bit pattern translation for FPGAs from a VHDL file will be proprietary to specific vendors. These translation tools also evolve with time. Are these translation tools considered trustable in the current scope of Case 3? If not, does the current scope include solving trust issues for these tools?

A: TRUST issues that impact the FPGA and the intermediate files are within scope.

Q: It is not clear from the BAA whether or not a Gold Standard GDS-II is available for Case 1 (un-trustable Fabrication Cycle).

A: A Gold Standard GDSII will be available for Case 1.

Q: Is Gold Standard chip or wafer available in addition to the chip with the Trojans in them (for both Case 1 and Case 2)?

A: A Gold Standard chip will be available for the appropriate test technique. Wafers will not be provided by the government.

Q: What is the timeline for getting Gold Standard design files (such as RTL, Verilog and GDS II files)? Can we get them at the beginning of the phases?

A: The appropriate Gold standard design files will be released approximately four months before the release of Test article 1-3 for the relevant experiments. Design files for Test article 0 are expected to be available shortly after the start of the program. Any additional requirements need to be defined in the proposal.

Q: Is EDIF netlist part of the standard design file?

A: EDIF netlists are part of the standard FPGA design files for Case 3.

Q: Please confirm that the sample test article-0 has no Trojans.

A: Test article-0 will have Trojans in it.

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Q: BAA specifies a maximum of 10 ICs to be available for each of the test articles (E1 through E3) that has Trojans in them. Will gold standard ICs (without Trojans) for E1 through E3 be provided as well – and if so how many?

A: There will be one gold standard IC made available.

Q: To do wafer level imaging, there is a need for wafers (instead of packaged ICs) – for both practice runs, calibration and for fault grading. Will these be provided and if so, how many? Are partial wafers (layer-by-layer) available?

A: No wafers will be provided. If wafers are required they must be priced into the proposal.

Q: One sample and three evaluation test articles are identified. Can we request/expect more experimental pre-fab test articles in the form of design files with Trojans for several test runs?

A: Any additional fab test runs needed must be listed and priced into the proposal.

Q: Do the Case 1, Case 2 and Case 3 – all use the same Test Articles and if so, how are they different in Trojan content (LD versus PD Trojans)?

A: The test articles for the various cases will be based on the same design. The ASIC and FPGA test articles will be different for the later phases. The Trojan content will different as well.

Q: The PIP language regarding teaming arrangements is unclear. Page 7 (Tech Areas 1 & 2) states "technology proposals that require multiple companies participating to succeed must have a teaming agreement..", and page 8 (Tech Area 3) states "A discussion in the proposal regarding the status of any such advanced teaming arrangements / relationships with potential component technology contractors shall be provided in response to this Technical Area.", however the following paragraph on page 8 states "A teaming arrangement/relationship between the technology providers and the SI contractor(s) is not a requirement of this BAA".

Establishing formal teaming agreements is a lengthy process and it would be difficult to finalize prior to a contract award. Are formal teaming agreements required for the proposal?

A: Given the inherent increase in risk associated with a team approach that is not structured as with a formal prime/sub arrangement, formal teaming agreement(s) must be provided as part of the proposal submission(s) in such instances. The lack of such agreements would be considered as an unacceptable level of risk during evaluations of Tech Area 1 and 2.

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Questions and Answers

Q: PIP section 9.6, page 27 states "Electronic proposals should be in Microsoft Word format or PDF". PIP section 16, page 42 states "The Contractor is required to provide four PowerPoint slides...", and Figure 19 on page 43 implies a desire for briefing text in the notes section of the slides.

Are the PowerPoint slides to be uploaded as a separate (.ppt) file?

A: Yes